WHAT IS CLAIMED:

1. A method, comprising:

sampling a program clock frequency at which information is sent over a communication link;

sampling a system frequency related to the communication link;

computing a result based on the sampled program clock frequency and the sampled system frequency; and

transmitting the result over the communication link.

2. The method of claim 1, wherein the sampling a sending frequency includes:

sampling a value of a counter counting the program clock frequency at a beginning and an end of a sampling interval.

3. The method of claim 1, wherein the sampling a system frequency includes:

sampling a value of a counter counting the system frequency at a beginning and an end of a sampling interval.

4. The method of claim 1, wherein the computing includes:

calculating a first difference value related to the program clock frequency, and

calculating a second difference value related to the system frequency.

5. The method of claim 4, wherein the computing further includes:

dividing the first difference value by the second difference value to obtain the result.

6. The method of claim 1, wherein the sampling a program clock frequency is triggered by the sampling a system frequency.

7. The method of claim 1, further comprising:

synchronizing the system frequency with a system frequency of a remote device via the communication link using a control protocol.

8. A method, comprising:

sampling a program clock frequency at which information received over a communication link is played;

sampling a system frequency related to the communication link;

computing a first value based on the sampled program clock frequency and the sampled system frequency;

receiving a second value via the communication link; and

adjusting the program clock frequency based on the first value and the second value.

9. The method of claim 8, wherein the computing includes:

calculating a first difference value related to the program clock frequency, and.

calculating a second difference value related to the system frequency.

10. The method of claim 9, wherein the computing further includes:

dividing the first difference value by the second difference value to obtain the first value.

11. The method of claim 8, further comprising:

generating a difference value from the first value and the second value,

wherein the adjusting adjusts the program clock frequency based on the difference value.

12. The method of claim 11, wherein the adjusting further includes:

changing a control voltage to an oscillator based on the difference value, or

changing a numerical value to adjust a frequency of a local program clock oscillator, or

changing a frequency of a virtual clock if data re-sampling is used in lieu of program clock adjustment.

13. The method of claim 8, wherein the second value indicates a sending frequency at which the received information is transmitted.

14. The method of claim 13, wherein the adjusting further includes:

increasing the program clock frequency if the first value and the second value indicate that the program clock frequency lags behind the sending frequency, and

decreasing the program clock frequency if the first value and the second value indicate that the sending frequency lags behind the program clock frequency.

15. The method of claim 13, where the adjusting includes:

re-sampling the information based on a difference between the first value and the second value.

16. A device, comprising:

a program clock to generate samples of information at a program frequency;

first circuitry to sample the program frequency of the program clock;

a system clock to generate a system frequency;

second circuitry to sample the system frequency of the system clock;

a processor to computationally combine the sampled program frequency from the first circuitry and the sampled system frequency from the second circuitry.

17. The device of claim 16, wherein the first circuitry includes:

a first counter to increment in accordance with the program frequency, and

a first register to store a value from the first counter.

18. The device of claim 16, wherein the second circuitry includes:

a second counter to increment in accordance with the system frequency, and

a second register to store a value from the second counter.

19. The device of claim 16, wherein the processor is arranged to divide the sampled program frequency by the sampled system frequency to generate a ratio.

20. The device of claim 19, wherein the processor is further arranged to send the ratio over a communication link to a receiver.

21. The device of claim 19, wherein the processor is further arranged to compare the ratio with another ratio received via a communication link from a transmitter.

22. The device of claim 21, wherein the processor is further arranged to adjust the program clock based on the ratio and the another ratio.

23. The device of claim 16, further comprising:

monitoring circuitry to trigger the first circuitry to sample the program frequency when the second circuitry samples the system frequency.

24. The device of claim 16, further comprising:

third circuitry to synchronize the system frequency with another system frequency in another device via a communication link.

25. A receiver, comprising:

a first clock to generate a first frequency;

a reference clock to generate a reference frequency;

a processor to combine information about the first frequency and information about the reference frequency, to receive information about a second frequency via a communication link with an unknown and variable transport delay, and to control the first clock based on the

information about the first frequency, the information about the reference frequency, and the information about the second frequency.

26. The receiver of claim 25, further comprising:

first circuitry connected to the first clock to generate the information about the first frequency; and

second circuitry connected to the reference clock to generate the information about the reference frequency.